Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) Device for writing data elements from a coprocessor into a FIFO memory, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:

a first counter for counting the available room in said FIFO memory;

a second counter for counting the number of data elements written into said FIFO memory;

control means coupled to the first and second counters, wherein the control means is configured for checking said first counter for available room in said FIFO memory, for checking said second counter whether a predetermined number N of data elements have been written into said FIFO memory, for decrementing the count of said first counter and for incrementing the count of said second counter after a data element has been written into said FIFO memory; and

output means for outputting data elements to said FIFO memory, wherein the output means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller;

wherein said control means is adapted to issue a first message when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory;

wherein said control means is adapted to issue a first call for available room in said FIFO memory to said controller; and

wherein said output means is adapted to forward said first message and said first call to said controller.

2. (previously presented) Device according to claim 1, wherein

said first message indicates that sufficient data elements have been written into said FIFO memory.

3. (previously presented) Device according to claim 2, wherein

said control means is further adapted to increment a write pointer, when data elements were output to said FIFO memory.

4. (previously presented) Device according to claim 3, wherein

said control means is further adapted to perform a wrap-around test after said write pointer was incremented.

5. (previously presented) Device according to claim 2, wherein

said control means is adapted to reset said second counter after issuing said first message.

6. (previously presented) Device according to claim 1, wherein

said control means is adapted to issue said first call for available room in said FIFO memory to said controller before said count of said first counter becomes zero.

7. (previously presented) Method for writing data elements from a coprocessor into a FIFO memory being in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said method comprising the steps of:

checking a first counter over a connection between a control means and the first counter, indicating the available room in said FIFO memory, in order to determine whether there is room available in said FIFO memory;

issuing over a connection between the control means and an output means a first call for available room in said FIFO memory;

forwarding over a connection between the output means and the controller the first call to said controller until there is room in said FIFO memory;

outputting data elements to said FIFO memory over a connection between the output means and the FIFO memory;

decrementing the count of said first counter after a data element has been written into said FIFO memory;

incrementing a second counter for counting the number of data elements written into said FIFO memory after a data element has been written into said FIFO memory;

checking said second counter over a connection between the control means and the second counter in order to determine whether a predetermined number N of data elements have been written into said FIFO memory; and

issuing over the connection between the control means and the output means a first message that sufficient data elements have been written into said FIFO memory when the count of said second counter has reached said predetermined number N by incrementing of the count of said second counter after a data element has been written into said FIFO memory.

8. (previously presented) Method according to claim 7, further comprising to step of:

incrementing a write pointer, when data elements were written into said FIFO memory.

9. (previously presented) Method according to claim 8, further comprising to step of:

performing a wrap-around test after said write pointer was incremented.

10. (previously presented) Method according to claim 7, further comprising to step of:

resetting said second counter after issuing said first message.

11. (previously presented) Method according to claim 7, further comprising to step of:

issuing said first call for available room in said FIFO memory to said controller before said count of said first counter becomes zero.

12. (previously presented) Device for reading data elements from a FIFO memory into a coprocessor, in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said device comprising:

a third counter for counting the available data elements in said FIFO memory;

a fourth counter for counting the number of data elements read from said FIFO memory;

control means coupled to the third and fourth counters, wherein the control means is configured for checking said third counter for available data element in said FIFO memory, for checking said fourth counter in order to determine whether a predetermined number N of data elements have been read from said FIFO memory, for decrementing the count of said third counter and for incrementing the count of said fourth counter after a data element has been read from said FIFO memory; and

input means for inputting data elements from said FIFO memory, wherein the input means comprises a first connection to the control means, a second connection to the FIFO memory, and a third connection to the controller, wherein the control means connects between the counters and the output means, and the output means connects between the control means and the controller;

wherein said control means is adapted to issue a second message when the count of said fourth counter has reached said predetermined number N by incrementing of the count of said fourth counter after a data element has been written into said FIFO memory;

wherein said control means is adapted to issue a second call for available data elements in said FIFO memory to said controller; and

wherein said output means is adapted to forward said second message and said second call to said controller.

13. (previously presented) Device according to claim 12, wherein

said second message indicates that sufficient data elements have been read from said FIFO memory.

14. (previously presented) Device according to claim 13, wherein

said control means is further adapted to increment a read pointer, when data elements were input from said FIFO memory.

15. (previously presented) Device according to claim 14, wherein

said control means is further adapted to perform a wrap-around test after said read pointer was incremented.

16. (previously presented) Device according to claim 13, wherein

said control means is adapted to reset said fourth counter after issuing said second message.

17. (previously presented) Device according to claim 13, wherein

said control means is adapted to issue said second call for available data elements in said FIFO memory to said controller before said count of said third counter becomes zero.

18. (previously presented) Method for reading data elements from a FIFO memory into a coprocessor being in a multiprocessing environment comprising at least one coprocessor, a FIFO memory and a controller, said method comprising the steps of:

checking a third counter over a connection between a control means and the third counter, indicating the available data elements in said FIFO memory, in order to determine whether there is data element available in said FIFO memory;

issuing over a connection between the control means and an input means a second call for available data elements in said FIFO memory;

forwarding over a connection between the input means and the controller the second call to said controller until there is a data element in said FIFO memory;

inputting data elements from said FIFO memory over a connection between the output means and the FIFO memory;

decrementing the count of said third counter after a data element has been read from said FIFO memory;

incrementing a fourth counter for counting the number of data elements read from said FIFO memory after a data element has been read from said FIFO memory;

checking said fourth counter over a connection between the control means and the fourth counter in order to determine whether a predetermined number N of data elements have been read from said FIFO memory; and

issuing over the connection between the control means and the input means a second message that sufficient data elements have been read from said FIFO memory when the count of said fourth counter has reached said predetermined number N by incrementing of the count of said fourth counter after a data element has been read from said FIFO memory.

19. (previously presented) Method according to claim 18, further comprising to step of:

incrementing a read pointer, when data elements were read from said FIFO memory.

20. (previously presented) Method according to claim 19, further comprising to step of:

performing a wrap-around test after said read pointer was incremented.

21. (previously presented) Method according to claim 18, further comprising to step of:

resetting said fourth counter after issuing said second message.

22. (previously presented) Method according to claim 18, further comprising to step of:

issuing said second call for available data elements in said FIFO memory to said controller before said count of said third counter becomes zero.

23. (previously presented) Multiprocessing computer system, comprising:

a FIFO memory;

at least one coprocessor;

a controller,

a device for writing according to claim 1.

24. (canceled)